Dual-Channel EEG Acquisition Circuit for Vehicular Safety System Based upon Brain-Computer Interface (BCI)

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Abstract: Electroencephalography (EEG) is the basis for many Brain Computer Interface (BCI) applications, where brain waves are captured, filtered, converted to digital form and analysed. In this paper we report on our design and implementation of wide-band dual-channel EEG acquisition circuit that is suitable for various Brain Computer Interface (BCI) applications. The advantages of the designed system include wide bandwidth covering frequencies from 0.2 up to 171 Hz, dual channel, 2 kHz sampling frequency, Analogue-to-Digital Conversion (ADC), simplicity and low cost. The designed EEG acquisition circuit was designed for BCI vehicular safety system, deep sleep and drowsiness detection applications that rely on analysing the lower frequency bands. However, the EEG acquisition circuit offers a wide bandwidth that makes it possible to analyse gamma brain waves that are related to spiritual and high concentration states of the brain. Compared to other EEG acquisition circuits that are limited to 46 and 100 Hz, our design offers greater bandwidth and resolution for high-frequency brain waves, which enables precise analysis of gamma signals. The designed circuit includes level shifter, limiter and ADC, which is driven by Field Programmable Gate Arrays (FPGA). The interface module with FPGA has been accomplished using a Finite State Machine (FSM), which drives the ADC chip and reads digital EEG data into FPGA. The sampling frequency is set at 2 kHz, which enables high grade BCI systems to be realised including clinical applications. Through the use of FPGA, the designed EEG acquisition circuit provides flexible and programmable DSP features, fast processing, accurate timing, stable sampling rate, and low-power consumption. Hardware Description Languages (HDL) such as VHDL and Verilog are the means to program and build various DSP modules inside FPGA.

Advanced DSP and control algorithms to be implemented with VHDL/Verilog, simulated and synthesised on FPGA are planned for future work.

Keywords: Brain-Computer Interface (BCI), Electroencephalography (EEG), Brain waves, Field Programmable Gate Arrays (FPGA), driver safety control modules, Digital Signal Processing (DSP).

دائرة اقتناء EEG مزدوجة القناة لنظام سلامة المركبات على أساس واجهة الدماغ والحاسب (BCI)

الملخص: تخطيط كهربية الدماغ (EEG) هو الأساس للعديد من تطبيقات واجهة الدماغ والحاسوب (BCI)، حيث يتم التقاط موجات الدماغ وتصفيتها وتحويلها إلى شكل رقمي وتحليلها. في هذا البحث نقدم تقريرًا عن تصميمنا وتنفيذنا لدائرة اكتساب EEG مزدوجة القناة عريضة النطاق مناسبة لمختلف تطبيقات واجهة الدماغ والحاسوب (BCI). تشمل مزايا النظام المصمم عرض نطاق واسع يغطي الترددات من ٠.٢ إلى ١٧١ هرتز، وقناة مزدوجة، وتردد العينات ٢ كيلو هرتز، والتحويل التناظري إلى الرقمي (ADC)، والبساطة والتكلفة المنخفضة. تم تصميم دائرة الاستحواذ EEG المصممة لنظام سلامة المركبات BCI وتطبيقات اكتشاف النعاس والنوم العميق التي تعتمد على تحليل نطاقات التردد المنخفضة. ومع ذلك، فإن دائرة اكتساب مخطط كهربية الدماغ توفر نطاقًا ترديدًا واسعًا يجعل من الممكن تحليل موجات الدماغ غاما المرتبطة بالحالات الروحية والتركيز العالي للدماغ. بالمقارنة مع دوائر اكتساب EEG الأخرى التي تقتصر على ٤٦ و١٠٠ هرتز، يوفر تصميمنا نطاقًا ترديدًا أكبر ودقة أكبر لموجات الدماغ عالية التردد، والتي تتيح التحليل الدقيق لإشارات غاما. تشتمل الدائرة المصممة على ناقل حركة المستوى والمحدد وADC، والتي يتم تشغيلها بواسطة مصفوفات البوابة القابلة للبرمجة الميدانية (FPGA). تم إنجاز وحدة الواجهة مع FPGA باستخدام آلة الحالة المحدودة (FSM)، التي تحركها شريحة ADC وتقرأ بيانات EEG الرقمية إلى FPGA. يتم ضبط تردد العينات على ٢ كيلو هرتز، مما يتيح تحقيق أنظمة BCI عالية الجودة بما في ذلك التطبيقات السريرية. من خلال استخدام FPGA، توفر دائرة الاستحواذ EEG المصممة ميزات DSP مرنة وقابلة للبرمجة، ومعالجة سريعة، وتوقيت دقيق، ومعدل أخذ عينات ثابت، واستهلاك منخفض للطاقة. لغات وصف الأجهزة (HDL) مثل VHDL وVerilog هي وسائل لبرمجة وبناء وحدات DSP مختلفة داخل FPGA.

DSP المتقدمة وخوارزميات التحكم التي سيتم تنفيذها باستخدام VHDL / Verilog ، يتم محاكاتها وتوليفها على FPGA ، مخطط لها للعمل في المستقبل.

1. Introduction

In this section we discuss the theory behind our designed EEG acquisition circuit. In section 1.1, we discuss brain waves and EEF artefacts. In section 1.2, we present BCI. In section 1.3, we discuss different types of EEG electrodes and their placement. In section 1.4, we present FPGA. In section 2, we present related work. In section 3, we present the details of the analogue front-end of the EEG signal acquisition module, which includes passive filters, Instrumentation Amplifier (In-Amp), active filtering and interfacing to the FPGA module. The tests and validation are presented in section 4. The conclusion and future work discussed in section 5.

1.1 Brain Waves

Brain waves are electro-magnetic signals that are commonly sinusoidal and their amplitudes range from 0.5 to 100 μV. Using Electroencephalography (EEG) [1], which enables recording brain waves related to brain activity through non-invasive techniques, with the electrodes placed along the scalp. Although invasive EEG techniques produce higher signal level compared to non-invasive EEG, invasive techniques require surgery and thus are not considered for their lack of versatility and added complexity to BCI systems. The EEG frequency spectrum includes frequency ranges starting from 0.2 Hz up to more than 100 Hz; the brain state of the individual may show certain frequencies more dominant. In this article, we designed and implemented a dual-channel EEG circuit that enables BCI applications that rely on the lower as well as the higher frequencies of the brain waves spectra. Deep sleep and drowsiness detection, for instance, rely on analysing the lower frequency bands, while the higher frequencies are related to high concentration and spiritual states of the brain. However, the circuit offers a wider bandwidth that makes it possible to analyse gamma brain waves that are related to spiritual and high concentration states of the brain. Compared to other EEG acquisition circuits that are limited to 100 Hz, our design offers greater bandwidth for gamma waves, i.e., up to 171 Hz, which enables precise analysis of gamma waves. The upper limit (171 Hz) for the bandwidth was chosen in order to avoid the higher harmonics of 60 Hz above 120 Hz, i.e., filtering only the 60 Hz and its first harmonic 120 Hz is necessary. Brainwaves have been categorised into five basic frequency bands. Studies have shown that certain activities can be correlated with increased in power for specific frequency ranges. For example, drowsiness and fatigue signs can be related to an increase in the θ frequency band from 4 to 8 Hz. An example of extracted θ waves in time domain is shown on Figure 1, which was acquired using our designed and built EEG acquisition circuit.

1.1.1 EEG artefacts

EEG artefacts describe signals, which are of non-cerebral origin. The amplitude of artefacts can be large relative to the size of amplitude of the cortical signals of interest. Some EEG artefacts are useful in various applications including Electrooculography (EOG), which enables detecting and tracking eye-movements. EOG is important in Polysomnography or sleep study, where it is used to diagnose sleep disorders, and is also used in EEG for assessing changes in alertness, drowsiness or sleep.

1.2 Brain-Computer Interface (BCI)

Brain Computer interface (BCI) is a technology that enables analysing brain activity or emotions using EEG and perform relevant actions based upon distinctive brain waves. This enables people with certain mobility issues or injuries to overcome restrictions and enhance their self-support. BCI is also employed in medical diagnosis against sleep disorders, drowsiness and certain brain issues.

1.3 EEG electrodes

EEG signals are picked up using electrodes using silver-plated electrodes. Special gel is usually used to ease electrical contact with the skin. Therefore, electrodes are to provide good electrical contact with skin. Different types of electrodes are available, some of which are disposable.

Reusable and disposable electrodes have been procured. The disposable type was not used since the number of electrodes was only enough for several trials.

Reusable electrodes can be utilised as dry or wet. Comprehensive comparison between dry and wet electrodes in [2] justifies the use of dry electrodes over wet electrodes. The following reusable electrodes have been considered:

1. Ag/AgCl hair penetrative electrodes, which are made of plastic material coated with a thin layer of silver.
2. Silver-plated cup dry electrodes.

After some experimentation, the hair penetrative electrodes have shown some wear signs, where the coating material was scratched off. Thus, we opted for the reusable silver plated cup electrodes (Ag) for their outstanding durability. To increase versatility, we have utilised the dry cup electrodes, i.e., without any gel or any additives.

1.3.1 Placement of electrodes

We have utilised two pairs of electrodes, i.e., two channels to capture brain waves. The number of channels determines the number of electrodes. Each channel requires one differential signal, which requires one pair of electrodes. In our design, we opted for a dual-channel circuit in

order to fulfil design constraints related to versatility and ease of use, which was confirmed using practical implementations of BCI systems. By using two channels only, the designed circuit has produced decent EEG signal quality that enabled the classification modules to achieve high accuracy.

Initial tests were made with dry electrodes [2] fixed using plaster tape on the forehead. Later on, a 3-D printed Ultracortex Mark IV frame available from OpenBCI provides good contact and support for the electrodes. The silver-plated electrodes were easy to fix on the front nodes of the frame. The electrodes of both channels on the frontal lobe are placed according to the 10-20 system as follows:

Channel 1: Differential input signal between Fp1 and Fp2 locations.

Channel 2: Differential input signal between the left ear clip and Fpz.

1.4 Field Programmable Gate Arrays (FPGA)

Field Programmable Gate Arrays (FPGAs) are Integrated Circuits (IC) that incorporate matrices of Configurable Logic Blocks (CLB) connected via programmable interconnects. Design on FPGAs can be reprogrammed or tuned many times to accomplish desired design improvement for. Programming an FPGA is accomplished through special Hardware Description Languages (HDL), such as VHDL [3]. The designed EEG circuit enables interface with FPGA, which has been accomplished using a Finite State Machine (FSM) in order to drive the ADC chip and read digital EEG data into FPGA. This makes the FPGA ready to implement DSP modules that we planned for future work.

2. Related Work

The work in [4] provides a single-channel low-cost EEG circuit for BCI system. Our work can be distinguished from the work in [4] in several aspects, with regard to simplicity and bandwidth, since our design is simpler with less amplification stages, without opto-coupling, without driven-right-leg (DRL) circuit and with a second additional channel.

The authors in [5] proposed a circuit design for extraction of EEG signals. Our work can be distinguished from their work in different ways; firstly, our design uses only one instrumentation amplifier per channel, which makes our design more cost effective. Another difference is that the total gain relatively high (10000-20000). We believe that excessive gain may lead to saturation and distortion due to exposure to noise signals.

In [6], a design of EEG signal acquisition system using Arduino MEGA1280 and EEG analyser is proposed. Our work can be distinguished from their work in different ways; firstly, our

design offers higher bandwidth (171 Hz). Secondly, our design proposes only 2 channels, compared to 16 channels, to increase versatility and ease of use.

The authors in [7], the authors propose an implementation of analogue portable EEG signal extraction system. Our work can be distinguished from the work in [8] in several aspects; firstly, we designed a 4th order active filters for the band-pass filters, which reduced the number of components. Although using higher order filters provides better rejection of unwanted frequencies, we opted for 4th order active filter since it requires only two op-amp stages, i.e., one chip of dual op-amp, which is enough to improve the SNR of the signal. Another reason, is the foreseen subsequent digital filtering on FPGA and software, which is more efficient. Secondly, the cut-off frequency of the system is limited to 100 Hz, whereas our design offers bandwidth covering frequencies between 0.18 and 171 Hz. Thirdly, we utilise a pair of 3.7 V batteries power source instead of dual 9 V, which means lower battery dimensions and weight. In [8], the authors propose a wireless 8-channel digital active-circuit EEG signal acquisition system that uses dry sensors. The total gain of the designed circuit in [8] is 9752, which is adequate and slightly higher than the gain of 9333 in our design. Generally, higher gain may lead to saturation and distortion of EEG signal. The bandwidth is 125 Hz compared to 171 Hz. The power supply is 3 V fed from 3.7 V batteries, while in our design we have dual 3.7 V power supply and 3.3 V for the ADC and digital interface. The analogue filters we have designed have a unity gain to simplify construction and reduce the number of components. Also this makes adjusting the gain at a single stage (the In-Amp, in our case). Another difference, is the number of channels is 2 in our design, while is it 8 in [8]. We believe that using 2 channels is sufficient for many BCI applications and offers more versatility. A final difference is cost, their circuit utilises compact modules, Flexible Printed Circuit Board (FPCB) and expensive In-Amp and op-amps, while we use inexpensive In-Amp and op-amps without FPCB.

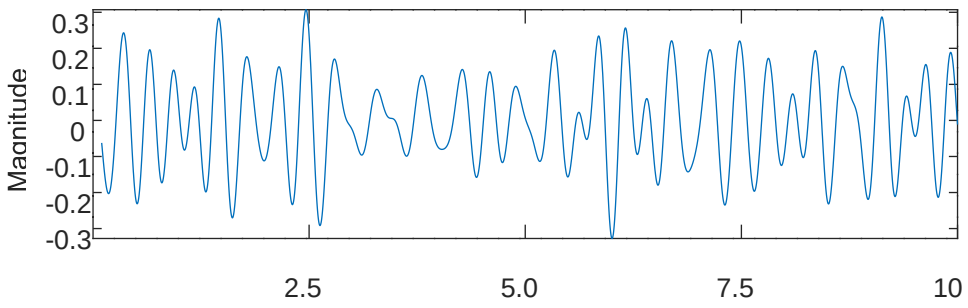

Figure 1: Theta waves (4-8 Hz) captured using the designed and built EEG acquisition circuit.

EEG headsets are available from different manufacturers notably OpenBCI [9] and Emotiv [10], of which the sampling frequencies are 250 and 128, respectively. The Emotiv products are intended only for personal use or research. At their best, the Emotiv cover the frequency range from 0.16 up to 45 Hz. Although the sampling rate is at best 8 kHz, it is down sampled to 128 Hz. Both sampling rates offer approximately the minimal acceptable rate of 2.5 times the highest frequency of interest [11].

On the other hand, since both types of headset are microcontroller-based, the sampling frequency drifts from the nominal value [10] since the hardware does not include a crystal oscillator. In our design, the use of FPGA board to drive the ADC eliminates these shortcomings of precise clock timing based upon a master crystal oscillator and dedicated Digital Clock Modules (DCM). Although most of the available headsets are adequate for research, they lack the precision for the higher frequency content of EEG waves due to the low sampling rate. We believe that the sampling frequency should be much more than double the highest frequency of the targeted signal. Therefore, the sampling frequency used in our design is 2 kHz, for it is more than 10 times the highest frequency component in our EEG system, i.e., 171 Hz. However, higher sampling rates of 2 kHz and even more are actually utilised in costly clinical EEG equipment.

Considering certain design objectives, the designs in [4], [5], [7], [8] and [9] fit into several application domains where they prove to be adequate, for example when the ease of use, cost and quick set-up are not mandatory. This includes BCI medical diagnosis equipment. However, our design objectives include BCI applications where cost, precision, small number of electrodes is preferred. For example, drowsiness detection and smart home control of are two major BCI applications that are targeted by our design objectives.

The number of channels was chosen based upon practical implementations of designs of a drowsiness-detection in vehicular safety system as well as other BCI applications, such as smart-home. In both applications, the dual-channel circuit have produced descent EEG signals that were successfully classified with high precision rates.

3. Analogue front-end of the EEG signal acquisition module

Our designed dual-channel EEG acquisition circuit is shown in Figure 4 is based upon Instrumentation Amplifier (In-Amp) circuit and different types of analogue filters to remove undesired noise. Level shifting and limiter circuit usually follow this circuit in order to convert the captured signal into digital form, i.e., Analogue-to-Digital Conversion (ADC), which enables Digital Signal Processing (DSP) that can be performed using FPGA or microcontroller.

An FPGA module has been successfully connected to the EEG circuit to drive the ADC chip and read EEG data into FPGA, which enables DSP modules to be implemented on FPGA. For the sake of brevity, the FPGA module is not explained in detail in this paper.

The dual-channel EEG acquisition circuit has been assembled on the Electronics Explorer board (available from Digilent), as shown in Figure 5, in order to profit from its integrated test bench for electronics projects. It includes mainly a 4-channel oscilloscope, multi-meter, signal generator, frequency spectrum analyser and different types of filters. The board was used to validate the EEG signals and export digital signals in data file for DSP using Octave, for example. The output of DSP can be viewed in Figure 6, where the attenuation due to the analogue Notch filter can be viewed around the 60 Hz point. The digital filtering effect of 60, 120 and 171 Hz is visible on the same figure with steep edges (clearly visible for the 120 and 171 Hz).

3.1 Passive LPF Since the required gain of the acquisition circuit is relatively high (several thousands), it is convenient to remove part of the undesired noise at the input of the In-Amp using a passive LPF with $f_c = 450\ Hz$ (composed of R1a1, R1b1, C1a1, C1b1 and C1b2, as shown in Figure 3) for both electrodes of channel 1. The value of f_c should be far from the frequencies of interest. For channel 2, the LPF is composed of R1a2, R1b2, C1b3, C1 and C1b4, as shown in

Figure 2. The values of R1b2 and R1a2 are tuned experimentally to produce most adequate results.

3.2 Instrumentation Amplifier (In-Amp) In-Amp is an electric circuit that is usually composed of 3 op-amps, of which two perform buffering with high-input impedance while a third op-amp serves as difference amplifier. The gain of In-Amp is determined by changing resistor R2a1, for channel 1 as shown on Figure 3).

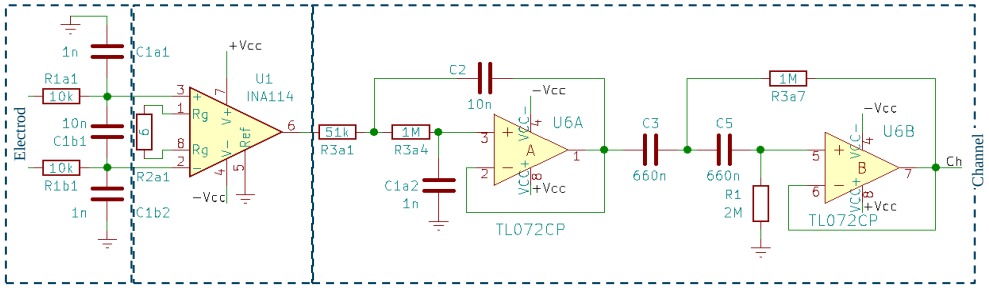

Figure 2: Main block diagram of the dual-channel EEG acquisition circuit.

The total gain of EEG acquisition circuits may be around 10000. We have designed the In-Amp circuit from scratch using two approaches; using discrete op-amps and using dedicated In-Amp chip, as shown in Figure 3. Although, the In-Amp with discrete op-amps produced

coherent EEG signals, high CMR, compactness and gain precision of dedicated In-Amp ICs, such as the INA114 IC, outperform In-Amp with discrete op-amps. Therefore, the INA114 In-Amp has been adopted in the final prototype as shown in Figure 3 as well as in

Figure .

The gain of the INA114 In-Amp for channel 2, as shown in

Figure 4, is determined by R2a3 6-Ω resistor, which produces gain around 9333. The presence of the preceding passive RC filter stage attenuates slightly the input signal.

3.3 Active filtering The raw EEG signals have low amplitude compared to surrounding noise, such as the 60-Hz fundamental frequency and its harmonics. Therefore, we have built double twin-T notch filter stage for channel 2 only, as shown in

Figure . For channel 1, the DSP module utilises Finite Impulse Response (FIR) digital filtering to remove the 60-Hz noise and its first harmonic, i.e., the 120-Hz. To tune the notch filter, we have connected resistors in series to get desired response. Channel 1 was designed such that it can be utilised in 50 or 60-Hz systems, since it does not include notch filters that undertake rejecting the 50 or 60-Hz power line noise.

Although test results showed that both channels offer good results, channel 2 offers better Signal to Noise Ratio (SNR) due to analogue filtering for the 60-Hz noise. Additional digital filtering can be applied to raw data using software or using FPGA in subsequent stages. The output of the oscilloscope can be exported to data file that can be processed using Octave to perform DSP. The frequency response of the EEG signal is shown on Figure 6, where the analogue filtering and digital filtering effects are visible. Obviously, the digital filtering using FIR filters is more efficient than analogue filtering.

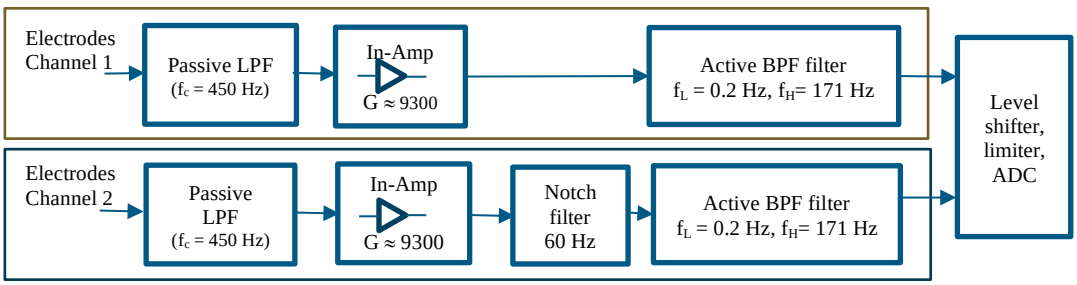

Figure 3: The schematic for channel 1 circuit showing the LPF, In-Amp and BPF.

Both channels contain BPF to further remove undesired frequencies outside of the 0.2-217 Hz frequency band. The design of active filters can be accomplished using online tools [12].

3.4 Interfacing with FPGA digital modules

Before feeding the analogue signals to the ADC, the level of the EEG signal should be shifted and limited within 0-3.3 V. This is accomplished using a level-shifter and limiter circuits to limit the signal below +3.3 V, which is the maximum supply voltage for the used ADC. For the sake of brevity, the schematic of this interfacing circuit is not shown in this context. The ADC enables further DSP processing in FPGA or microcontroller in order to perform additional complex analysis operations, such as Fourier and Wavelet transforms.

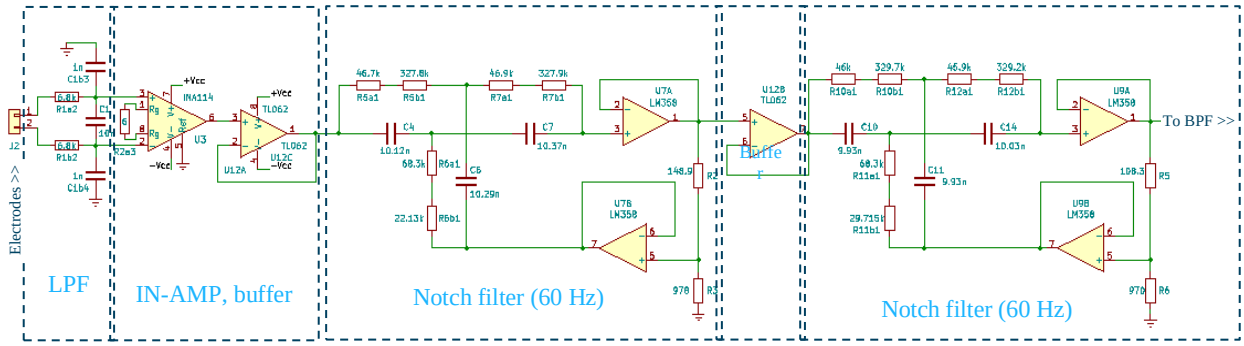

Figure 4: The schematic for channel 2 circuit showing the LPF, In-Amp and 60-Hz Notch filters.

4. Tests and validation results

We have performed several test scenarios for the various sections of the designed circuit. The notch filters are sensitive part to resistors. The test scenarios were performed during the breadboard early phase and after building the prototype on PCB, which is shown on Figure 7.

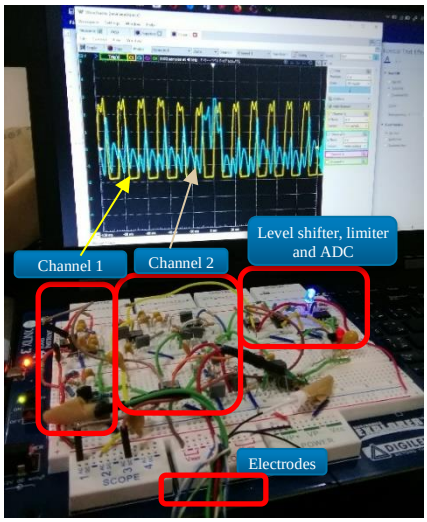

Figure 5: Testing the dual-channel EEG acquisition circuit using oscilloscope during early design phase.

A sample output of captured EEG signals for both input channels is shown on Figure 5, which describes the output of both channels 1 and 2 in time domain, while Figure 8 shows the frequency spectrum of channel 2 as viewed on the oscilloscope, which shows clearly the effect of the analogue filters used; the magnitude of the 60 Hz is less than that for 120 Hz and beyond 120 Hz the effect of LPF is visible. On the same figure, the harmonics of 60 Hz are visible with peaks at 120, 180, 240, 300 and 360. Since the frequency range of interest is below 171 Hz, we have to deal only with 60 and 120 Hz.

After the analogue circuitry was validated, the first PCB prototype was designed and manufactured. Eventually, the EEG board was successfully integrated with BCI applications that take the output data of the EEG board and process it offline in order to perform training of different classification modules. Using the built circuit, a considerable dataset of recordings was established over several months for several persons and different classes related to brain activity. For the sake of brevity, the details of the designed BCI applications are left to future article of ours.

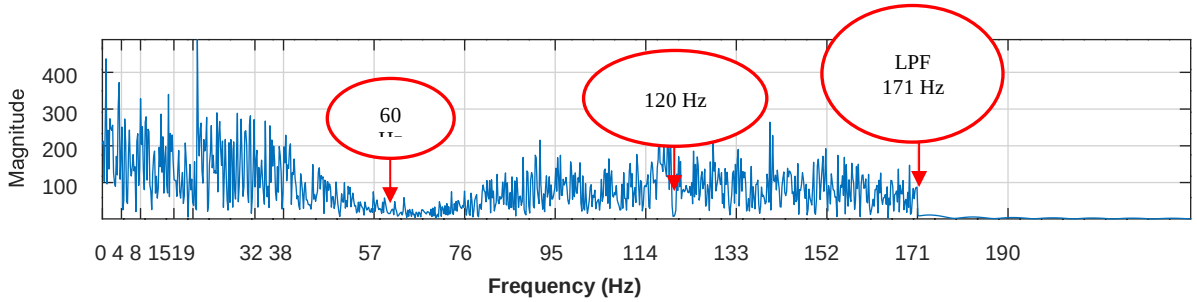

Figure 6: Frequency spectrum showing removal of the 60 and 120 Hz noise and frequencies beyond 171 Hz.

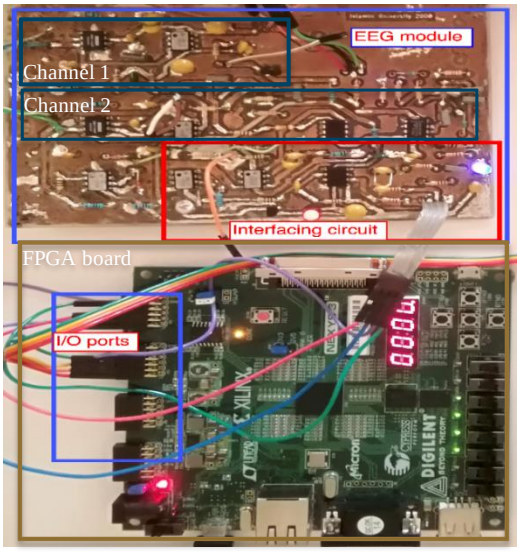

Figure 7: PCB of the designed EEG acquisition circuit connected to FPGA board

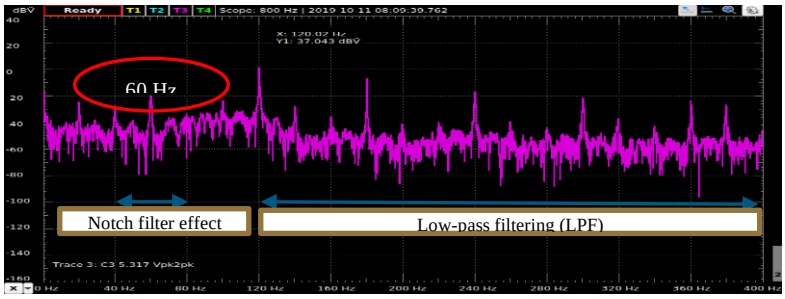

Figure 8: Frequency response, showing the attenuation of the 60 Hz signal and the effect of the BPF.

5. Conclusion

EEG signals are employed in many BCI applications including driver safety, smart-home

Figure 8: Frequency response, showing the attenuation of the 60 Hz signal and the effect of the BPF.

control and medical diagnosis. We have demonstrated our design and implementation of a dual-channel EEG acquisition. Channel 1 does not include notch filters, thus it can be used in 50 and 60-Hz power systems, while channel 2 offers active notch filters to attenuate the 60-Hz noise. The built EEG acquisition prototype is based upon dedicated In-Amp that is followed by BPF and Twin-T notch active filters. The output of the analogue circuit is connected to ADC circuitry that is controlled by FPGA, which enables further DSP modules to be designed and implemented on FPGA. The interface with FPGA kit has been designed, and implemented using FSM.

The advantages of the designed circuit include wide bandwidth covering frequencies from 0.2 up to 171 Hz, dual channel, flexible sampling frequency (2 kHz is recommended), ADC conversion, compliance with 50 and 60 Hz power systems, precise timing and sampling rate, simplicity and low cost.

Introducing programmable DSP features can be accomplished using FPGA that provide flexible and powerful platforms for DSP that employ parallelism and offer low-power consumption. Hardware Description Languages (HDL) such as VHDL and Verilog are the means to build modules inside FPGA. Algorithms of control modules can be implemented with VHDL/Verilog, simulated and synthesised on FPGA.

To fully test the EEG acquisition circuit, it has been manufactured on PCB, integrated with different classifier modules for a drowsiness-detection vehicular safety BCI system as well as smart-home control. Test result were coherent and proved the soundness of design, which are detailed in other articles of ours. The designed EEG acquisition circuit enables the design and development of other BCI systems, such as medical diagnosis for sleep disorders.

All test scenarios were successful, a prototype PCB was built and the interface module with FPGA has been completed and prepared for further DSP modules to be realised.

The future improvements to the circuit include using quad op-amps, integration of complex DSP modules on FPGA and integrate a wireless module to communicate with BCI systems using Wi-Fi or Bluetooth.

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