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A switching-loss reduction strategy for improving the efficiency of three-level inverters

Sid-Ahmed Touil [1*], Nasserdine Boudjerda [2], Hemza Gueddar [3],

[1] Institute of Electrical and Electronic Engineering, University M'hamed Bougara. Boumerdes, Algeria, s.touil@univ-boumerdes.dz

[2] Renewable Energy Laboratory, University of Jijel, Algeria, n_boudjerda@yahoo.fr

[3] Electrical Engineering department, University of Jijel, Algeria, hamza01gueddar@gmail.com

*Corresponding author: (Sid-Ahmed Touil), *Email Address*: s.touil@univ-boumerdes.dz

Abstract

This paper investigates a generalised discontinuous pulse width modulation (DPWM) technique designed to minimise switching losses in three-level inverters. The proposed approach addresses one of the primary sources of power loss in multilevel power converters by strategically reducing the number of commutations per switching period. The study compares the performance of various DPWM strategies with that of the conventional hybrid space vector modulation (HSVM) method using detailed MATLAB/Simulink simulations. The results show that switching losses can be significantly reduced by a third compared to the classical PWM technique. However, the proposed technique leads to a deterioration in Total Harmonic Distortion (THD) relative to the conventional method, while staying within acceptable operational standards. These findings highlight the capability of the proposed technique to effectively balance inverter efficiency and output waveform quality. The proposed method presents a promising way to enhance the performance of high-power and high-efficiency applications, such as motor drives and renewable energy conversion systems.

Keywords: Three-phase inverters; Space Vector Modulation; Discontinuous Pulse Width Modulation (PWM); switching losses; Total Harmonic Distortion (THD).

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1. Introduction

Inverters are controllable voltage sources that can generate output waveforms with specific frequencies, amplitudes, and harmonic characteristics. They play a crucial role in power conversion systems by supplying alternating current from direct current sources while maintaining the desired voltage and frequency. According to their structure, inverters are bidirectional and are typically composed of switching cells that enable current to flow in both directions. Depending on the intended application, additional filtering components may be required to improve waveform quality.

Today, inverters are widely used in a variety of modern technologies, including electric and hybrid vehicles, renewable energy systems such as photovoltaics and wind power conversion, uninterruptible power supplies, and advanced industrial automation. Their flexibility and efficiency make them an essential component in the transition towards smart, energy-efficient and electrified systems.

For high-power and medium-voltage applications, the three-level inverter topology offers several advantages over conventional two-level structures. This configuration significantly reduces harmonic distortion in both the output voltage and current, often eliminating the need for bulky output filters. Furthermore, each semiconductor device is subjected to only half of the DC-link voltage, which reduces switching stress and enables the use of lower-rated components. Consequently, overall efficiency improves, switching and thermal losses are minimised, and the size and cost of cooling systems are reduced. Although several studies have examined modulation strategies for two level inverters, most works have focused on classical SPWM or SVM approaches [1-4], providing limited insight into the practical implementation of DPWM schemes [1]. Existing contributions usually address switching loss reduction or provide theoretical comparisons, but rarely investigate the impact of DPWM on harmonic quality, switching behavior.

Advanced modulation techniques such as Discontinuous Pulse Width Modulation (DPWM) have been developed to further enhance inverter performance. The aim of these techniques is to reduce the number of switching events per cycle, thereby minimizing switching losses without significantly deteriorating waveform quality. This study analyses and compares different DPWM strategies with the conventional Hybrid Space Vector Modulation (HSVM) approach. Particular attention is given to assessing their impact on inverter efficiency and total harmonic distortion (THD).
The remainder of this paper is organized as follows:
Section II introduces the principles of SVM and its hybrid (HSVM). Section III presents the implementation of various DPWM strategies. Section IV discusses the simulation setup and results. Section V concludes the paper by presenting key findings and offering perspectives for future research.

2. SVM and Hybrid SVM relationship

The SVM technique is a modulation method with high linearity performances and good spectral properties. It is based on a complex representation of the inverter output voltage and allows a direct calculation of the inverter switching times, therefore the obtained reference voltage vector, rotates in the complex plan [1-3] is given by:

$$\overrightarrow{V_{qd}^*} = V_q^* - jV_d^* \tag{1}$$

Where:

$$V_q^* = \frac{1}{3}\left(2V_a^* - V_b^* - V_c^*\right) \tag{2}$$

$$V_d^* = \frac{\sqrt{3}}{3}\left(V_c^* - V_b^*\right) \tag{3}$$

The rotating vector $\overrightarrow{V_{qd}^*}$ defines eight state vectors (V_0, V_1 ...V_7); V_0 and V_7 are called zero state vectors and the six others define six sectors subdivided in sampling periods T_s in which is assumed constant. In each sector, two adjacent vectors are active during T_1 and T_2 respectively [1-3]:

$$T_1 = T_s\frac{\sqrt{3}}{2}\left(V_d^*\cos\left(n\frac{\pi}{3}\right) + V_q^*\sin\left(n\frac{\pi}{3}\right)\right) \tag{4}$$

$$T_2 = -T_s\frac{\sqrt{3}}{2}\left(V_d^*\cos\left((n-1)\frac{\pi}{3}\right) + V_q^*\sin\left((n-1)\frac{\pi}{3}\right)\right) \tag{5}$$

n: sector number (n = 1… 6).

Zero state vectors V_7 and V_0 are active during k_0T_0 and $(1-k_0)T_0$ respectively, with ($0 \le k_0 \le 1$). The total duration T_0 is given by:

$$T_0 = T_s - T_1 - T_2 \tag{6}$$

For the classical SVM, k_0 = 0.5, therefore V_7 and V_0 have the same durations:

$$k_0T_0 = (1-k_0)T_0 = T_0/2 \tag{7}$$

In practice, the SVM switching signals can be generated either by space vectors or by comparison of three reference signals with a triangular carrier, exactly in the same way of the sinusoidal modulation (SM); the only difference is in the reference signals. This last method is called hybrid SVM (HSVM) and the appropriate reference signals can be obtained by adding a zero-sequence signal to the sinusoidal ones as follows [4]:

$$v_{abc}^{**} = v_{abc}^{*} + v_{zs}^{*} \tag{8}$$

Where, v_{abc}^{*} is the vector of reference signals for sinusoidal modulation (SM), i.e. wanted output voltages and v_{zs}^{*} is the zero sequence given by [4]:

$$v_{zs}^{*} = -\left[(1-2k_0) + k_0 v_{\max}^{*} + (1-k_0)v_{\min}^{*}\right] \tag{9}$$

For the classical SVM, vectors V_0 and V_7 have equal durations (k_0 = 0.5), Where $v_{\min}^{*}$, v_{mid}^{*} and $v_{\max}^{*}$ are minimum, middle and maximum values of reference signals [1, 2].

3. Generalized Discontinuous PWM

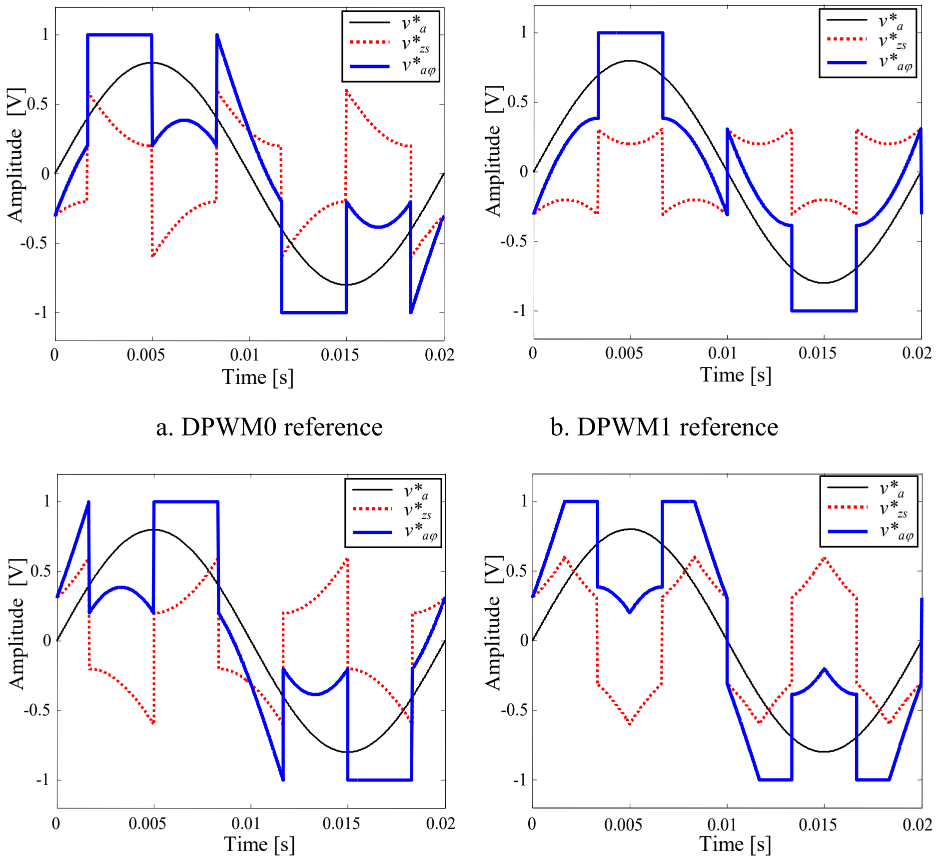
The principle of generalized discontinuous PWM (GDPWM) technique is based on the injection of a zero sequence v_{zs}^{*} to the sinusoidal references v_{abc}^{*} in the same way of HSVM. Where the only difference is in the derivation of the zero sequence. The main goals of this technique are:

- Reducing the number of switching by 1/3 symmetrically in the two half cycles: all switches are inactive during a phase angle of $\pi/3$. This is the purpose of this technique because it allows a reduction of the switching losses in the same ratio while conserving a symmetrical operation of all switches [4].
- Extending the linearity up to $2/\sqrt{3}$ as in the third harmonic injection and HSVM.

In order to generate the various GDPWM algorithms, we consider the initial vector v_{abc}^{*} of reference signals for the classical PWM technique using sinusoidal modulation. Then we use the new vector of references, $v_{abc\varphi}^{*}$ phase is shifted of the initial vector v_{abc}^{*}, by φ $(0 \le \varphi < \pi/3)$. For each value of the delay $(0 \le \varphi < \pi/3)$, the maximum and minimum values of $v_{abc\varphi}^{*}$ can be obtained as: $V_{\max,\varphi} = \max(v_{abc\varphi}^{*})$ and $V_{\min,\varphi} = \min(v_{abc\varphi}^{*})$. Finally, the zero sequence v_{zs}^{*} is built using expression (9), in which the parameter k_0 takes alternately the values *0* or *1* as follows [4]:

$$\begin{cases} if \;\; V_{\max,\varphi} + V_{\min,\varphi} < 0 \;\; \text{then}: k_0 = 1 \\ if \;\; V_{\max,\varphi} + V_{\min,\varphi} \ge 0 \;\; \text{then}: k_0 = 0 \end{cases} \tag{10}$$

Various DPWM modulating waveforms can be generated by using $(0 \le \varphi < \pi/3)$. The particular cases of φ equals to $0, \pi/6$, $\pi/3$ and $\pi/2$ are called DPWM3, DPWM0, DPWM1 and DPWM2 respectively [5, 6]. For these particular schemes, the initial sinusoidal reference phase voltage, the zero sequence signal and the final reference phase voltage (modulating waveform) are shown in Figure 1, considering the modulation ratio r = 0.8.



a. DPWM0 reference b. DPWM1 reference

a. DPWM2 reference b. DPWM3 reference

Fig. 1. Modulation principale of HSVM

4. Simulation results

The structure of the three-level neutral point clamped (NPC) inverter is presented in (Fig.2). Each of the three legs is connected to two series diode and incorporates four main power switch devices with anti-parallel diode in series as shown in Figure 2.

Each inverter leg requires four control signals [7]:

$$q_{i3} = 1 - q_{i1} \quad \text{and} \quad q_{i4} = 1 - q_{i2},\ t = 1,2,3 \tag{11}$$

For the leg 1, q_{11} is obtained by comparing the reference signal to the upper carrier and q_{12} is obtained by comparing the same reference to the lower carrier, while q_{13} and q_{14} are obtained using (10). All switches operate symmetrically, hence our study is restricted to q_{11} only [7-9].

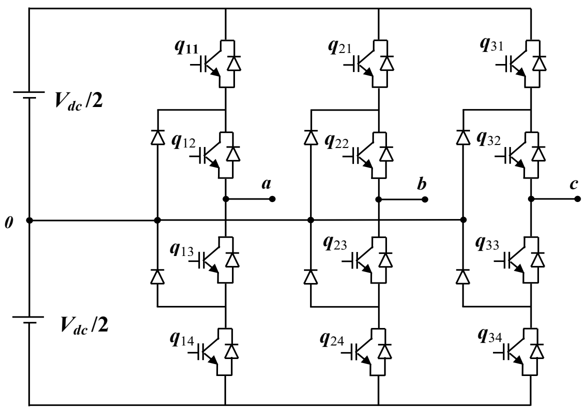
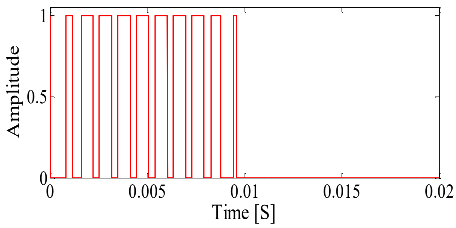
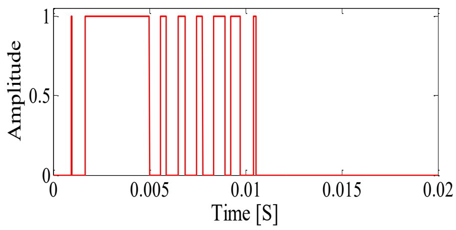


Fig. 2. Modulation principale of HSVM

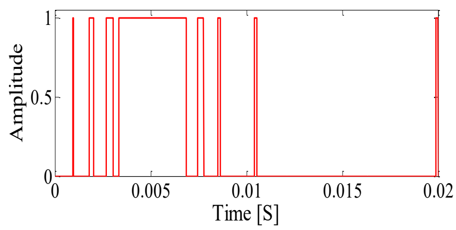
Figure 3 illustrates the control signals generated for the various DPWM schemes at a modulation index (M = 0.8) and a frequency ratio (r = 21). It can be observed that each modulation strategy exhibits distinct switching patterns, corresponding to different intervals of zero-sequence application, which directly influence the inverter's switching behavior and overall efficiency.



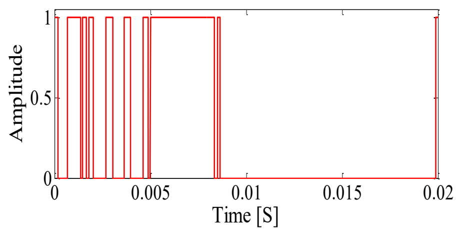
a. HSVM



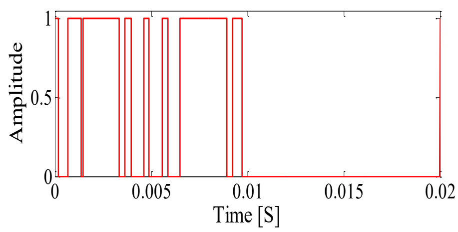
b. DPWM0



c. DPWM1



b. DPWM2

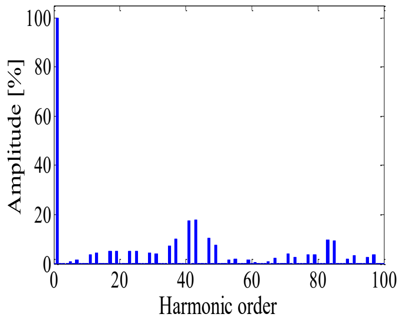


c. DPWM3

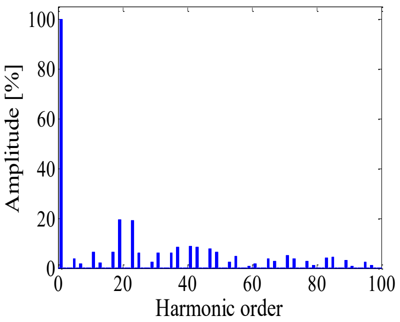
Fig. 3. Control signals for various DPWM schemes (r = 0.8 and M = 21)

Figure 4 presents the harmonic spectra of the inverter output voltage under the same operating conditions (r = 0.8, M = 21), with various PWM techniques. The spectra clearly show that the proposed

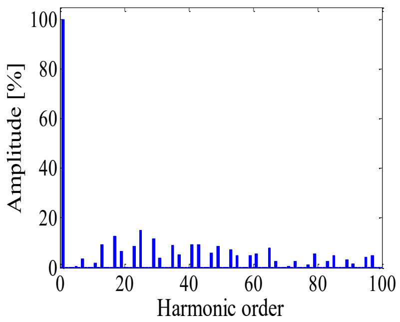
DPWM methods effectively reduce low-order harmonics while maintaining an acceptable total harmonic distortion (THD) level, confirming their ability to improve waveform quality and converter performance.



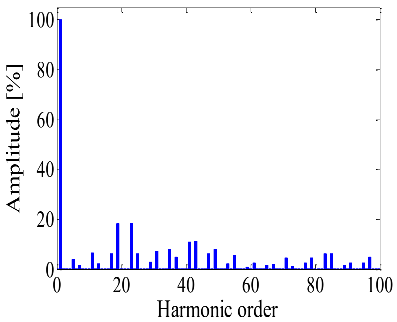
a. HSVM



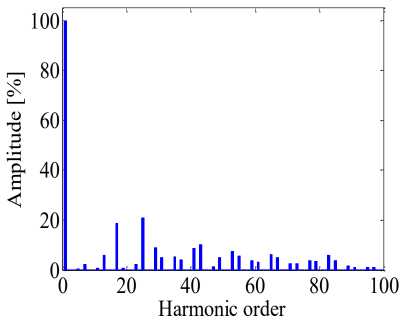
b. DPWM0



c. DPWM1



d. DPWM2



e. DPWM3

Fig. 4. Harmonic spectra of output voltage ($r = 0.8$ and $M = 21$)

Table 1 summarizes the performance comparison of the proposed Discontinuous Pulse Width Modulation (DPWM) schemes, DPWM0, DPWM1, DPWM2, and DPWM3 with the conventional Hybrid Space Vector Modulation (HSVM) method for a three-level NPC inverter. The parameters considered include the number of commutations per switching period, the Total Harmonic Distortion (THD), and the Weighted Total Harmonic Distortion (THDW) of the output voltage.

Table 1. Comparison of DPWM schemes for three-level inverter

PWM Technique	Number of commutations per period	THD (%)	THDW (%)
HSVM	21	42.64	1.05
DPWM0	16	42.07	1.70
DPWM1	16	42.47	1.49
DPWM2	18	43.94	1.65
DPWM3	16	42.93	1.53

Notes:

1. The THD is the total harmonic distortion defined as follows:

$$THD(V) = \frac{\sqrt{\sum_{n=2}^{\infty} V_{neff}^{2}}}{V_{1eff}}$$

2. The THDW is the weighted total harmonic distortion defined as follows:

$$THDW(V) = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{V_{neff}}{n} \right)^{2}}}{V_{1eff}}$$

It important indices to measure quality of output voltage fed to grid, gives a better measure of harmonic pollution by using the order of each harmonic component as its weight factor.

It can be observed that all DPWM techniques significantly reduce the number of commutations per period compared to HSVM. Specifically, DPWM0, DPWM1, and DPWM3 achieve approximately 30% reduction in switching sequences, while DPWM2 exhibits a smaller decrease. This reduction directly contributes to lower switching losses and improved inverter efficiency.

Regarding harmonic performance, the THD values of all DPWM strategies remain comparable to that of HSVM, with only minor variations within ± 2%. Although the weighted distortion (THDW) slightly increases for the DPWM methods, it remains within acceptable limits for most high-power applications. These results demonstrate that the DPWM techniques effectively reduce switching losses without significantly compromising the quality of the output voltage, confirming their potential for efficient multilevel inverter operation.

Figure 4 illustrates the harmonic spectra of the inverter output voltage, which further validates these findings. The spectra show that the DPWM schemes have similar harmonic profiles to the HSVM scheme, with the dominant harmonics shifted to higher frequencies that can be filtered more easily if required. This confirms that the proposed DPWM strategies achieve an excellent balance between reduced switching activity and acceptable harmonic performance.

5. Conclusion

This paper presents a detailed comparative study of a three-level inverter operating under various advanced discontinuous pulse width modulation (DPWM) strategies, specifically DPWM0, DPWM1, DPWM2 and DPWM3 and benchmarks them against the conventional hybrid space vector modulation (HSVM) approach. The main aim was to minimise inverter switching losses by reducing the number of commutations during each switching cycle. The simulation results demonstrate that the proposed DPWM techniques achieve a significant reduction in switching losses while maintaining acceptable total harmonic distortion (THD) in the output voltage.

These results confirm the effectiveness of DPWM strategies in improving inverter efficiency and thermal performance without compromising the quality of the output waveform. Consequently, the proposed control schemes offer a promising alternative for high-efficiency power conversion in applications such as electric drives, renewable energy systems, and medium-voltage converters.

Future research will focus on experimentally validating these modulation strategies using a hardware prototype to verify their real-time performance. Further investigations may involve optimising DPWM switching sequences under dynamic load conditions and extending the approach to multilevel topologies with more than three voltage levels, with the aim of further improving energy efficiency and harmonic quality.

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